REMARKS

This Amendment amends Claims 1, 11, and 15, the Title of the application and, cancels Claim 17. Now in the application are Claims 1-16 and 18-20 of which Claims 1, 9, 11, and 16 are independent. The following comments address all stated grounds for rejection, and place the presently pending claims, as identified above, in condition for allowance.

Objection to Specification:

The title to the invention is objected to as non-descriptive. The foregoing amendment amends the title of the application to Microprocessor and Method for Out of Order Simultaneous Multi-Threading, which the Applicants submit is descriptive of the invention. Accordingly, Applicants respectively request the Examiner to reconsider and withdraw the objection to the specification.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

Claims 1, 2, 3, 6, 8-13, and 16-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,092,175 of Levy et al. (hereinafter "Levy"). For the ease of the discussion of the claim rejections under 35 U.S.C. §102, each claim set is discussed separately below.

IA. Rejection of Claims 1, 2, 3, 6, and 8 Under 35 U.S.C. §102(b):

Claims 1, 2, and 3 stand rejected under 35 U.S.C. §102(b) as being anticipated by Levy. Applicants respectively traverse this rejection based on the above amendments and contend that Levy does not anticipate Claims 1, 2, 3, 6, and 8.

Claims 2, 3, 6, and 8 depend directly or indirectly upon amended independent Claim 1, and therefore incorporate the patentable features of Claim 1.

Amended Claim 1 is directed to a microprocessor that includes a first register file containing registers and a second register file containing registers. The microprocessor further includes a facility for granting access to the first and second register files in a

single-thread mode and in a multi-thread mode. In the single-thread mode, a register name is renamed to refer to a first location in the first register file and to a first location in the second register file and a single-thread has access to both the first register file and the second register file. In the multi-thread mode, the register name refers to one location in one of the first register file and the second register file, and a first thread has access to the first register file and a second thread has access to the second register file.

A benefit of the structure of the microprocessor in amended Claim 1 is the performance of the processor in the single-thread mode. That is, in the single-thread mode, the single-thread has access to the first register file and the second register file to maximize a peak issue rate. Thus, the microprocessor of amended Claim 1 has a structure that seeks to maximize the issue rate of instructions per cycle.

The Levy reference does not anticipate amended Claim 1. The Levy reference is directed to the organizing of processor register storage so as to reduce the number of registers required and to increase the performance of a given number of registers. More specifically, the Levy reference discloses a method for allocating unused registers assigned to an idle context for use by the active contexts in a multi-threaded processor that is capable of executing instructions from a plurality of threads out of order. At least some of these registers are usable as renaming registers. The renaming registers are dynamically allocated and assigned to a thread being processed by the multi-threaded processor, as required to support out of order execution of instructions for the thread.

The Levy reference does not disclose a facility for granting access to the first and second register files in a single-thread mode and in a multi-thread mode as recited in amended Claim 1. Moreover, nowhere does the Levy reference disclose that in the single-thread mode, a register name is renamed to refer to a first location in the first register file and to a first location in the second register file. Further, the Levy reference does not disclose, inherently or otherwise, that in the multi-thread mode a register name refers to one location in one of the first register file and the second register file. The structure, function and operation of the microprocessor of amended Claim 1 optimizes performance of the single-thread mode and allows a maximum peak issue rate in such instances.

In contrast to amended Claim 1, the Levy reference discloses a semi shared architectural and shared renaming (SSASR) registers. This register resource configuration scheme of Levy is based on the observation that a parallel program might execute on a simultaneous multi-threading processor with fewer threads than the number of hardware context. In this situation, the architectural registers for the idle hardware context might go unused. In the SSASR scheme taught by Levy, the architectural registers of the idle context are usable as renaming registers for any loaded context, that is, they may be used as renaming registers for the context of an active thread. More specifically, the per thread registers for the unused thread contexts (those currently not loaded with executing threads) are used as renaming registers, i.e. to be shared among the multiple executing threads, along with the dedicated shared renaming registers, and allocated in the same manner as the shared renaming registers. Therefore, in the SSASR scheme, cited by the Examiner, if fewer threads are executing then the maximum supported by the processor, those fewer threads can benefit from additional renaming registers (i.e. the "private" architecturally specified registers of the idle threads) that would not be available in another scheme.

The Levy reference does not disclose a microprocessor with a single-thread mode where a register name is renamed to refer to a first location in a first register file and to a first location in a second register file. In other words, in the single-thread mode of the microprocessor of amended Claim 1, a single register name is renamed to refer to two locations, one location in a first register file and one location in a second register file. Nowhere does the Levy reference disclose such a feature. The Levy reference is concerned with making available unused registers allocated to threads that are not currently executing. In this manner, Levy increase the number of registers available to executing threads. However, the Levy reference does not disclose that in a single-thread mode a register named is renamed to refer to a first location in a first register file and to a first location in a second register file. Hence, the Levy reference does not anticipate Amended Claim 1 and therefore does not anticipate Claims 2, 3, 6, and 8.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 1, 2, 3, 6, and 8 under 35 U.S.C. §102(b).

IB. Rejection of Claims 9 and 10 Under 35 U.S.C. §102(b):

Claims 9 and 10 stand rejected under 35 U.S.C. §102(b) as being anticipated by Levy. Applicants respectfully traverse this rejection and contend that Levy does not anticipate Claims 9 and 10.

Claim 10 depends from independent Claim 9, and therefore incorporates the patentable features of Claim 9.

Claim 9 is directed to a mapping mechanism in a microprocessor having a first register file and a second register file. The mapping mechanism is for mapping references in instructions to registers in both the first register file and the second register file when in a single-thread mode; and for mapping references to registers in instructions to a first thread solely to registers in the first register file and references to registers in instructions in a second thread to registers in the second register file when in a multi-thread mode. The Levy reference does not anticipate Claims 9 and 10.

The Levy reference discloses a simultaneous multi-threading microprocessor that reallocates registers allocated to a thread that is not executing to a thread that is executing. The Levy reference discloses a register handler that implements the mapping of references to architecturally specified registers to specific renaming registers. The Levy reference further discloses that architecturally registers of an idle context are useable as renaming registers for any loaded context, e.g., they may be used as renaming registers for the active context. More specifically, the Levy reference discloses a scheme to increase the number of renaming registers available to active context based on architectural registers associated with an inactive context.

In contrast to Levy, Claim 9 discloses a microprocessor having a first register file, a second register file, and a mapping mechanism for mapping references to registers in instructions to both the first register file and the second register file when in a single-thread mode. Further, in a multi-thread mode the mapping mechanism can map references to registers in instructions of a first thread solely to registers in the first register file and references to registers in instructions in a second thread to registers in the second register file. The Levy reference does not disclose a mapping mechanism for

mapping references to registers in instructions to both the first register file and the second register file when in a single-thread mode.

In contrast, the Levy reference discloses the ability to increase the number of available renaming registers under certain operating conditions. Nevertheless, the Levy reference does not disclose a mapping mechanism for mapping references to registers in instructions to both the first register file and the second register file when in a single-thread mode. Hence, in accordance with the microprocessor and the mapping mechanism of Claim 9, in the single-thread mode a first register from the first register file and a first register from a second register file hold identical content. Hence, the microprocessor of Claim 9 has a structure, and an operation and a function different from that of the microprocessor disclosed by the Levy reference. Accordingly, the Levy reference does not anticipate Claims 9 and 10.

Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 9 and 10 under 35 U.S.C. §102(b).

IC. Rejection of Claim 11-13 Under 35 U.S.C. §102(b):

Claims 11-13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Levy. Applicants respectfully traverse this rejection based on the above amendments and the below arguments, and contend that Levy does not anticipate Claims 11-13 as amended.

Claims 12 and 13 depend directly or indirectly upon amended independent Claim 11 and therefore incorporate the patentable features of amended Claim 11.

Amended Claim 11 is directed to a method performed in a microprocessor having multiple register sets. The method includes, amongst other steps, a step of switching from a multi-thread mode to a single-thread mode where a single-thread is executing. In the single-thread mode, a single register name is renamed to refer to a location in each respective ones of the register sets. The Levy register does not disclose such a step and therefore fails to anticipate Claims 11-13 as amended.

The Levy reference is concerned re-allocating unused architectural registers as renaming registers. Nowhere does the Levy reference disclose a microprocessor having a

single-thread mode where a single-thread is executing, and wherein in the single-thread mode a single register name is renamed to refer to a location in each respective ones of the register sets. That is, in the single register mode recited in amended Claim 11 a single register name is renamed to refer to one location in a first register file and one location in a second register file. Nowhere, does Levy disclose such a feature. Levy discloses increasing the amount of available renaming registers using architectural registers from idle context. Nowhere does the Levy reference disclose in a single-thread mode a single register name is renamed to refer to two locations in separate respective ones of multiple register sets. Hence, the Levy reference does not anticipate amended Claim 11.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 11-13 under 35 U.S.C. §102(b).

ID. Rejection of Claims 16-20 Under 35 U.S.C. §102(b):

Claims 16-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Levy. Applicants respectfully traverse this rejection based on the above amendments and the below arguments, and contend that Levy does not anticipate Claims 16-20, as amended.

Claims 17-20 depend directly or indirectly upon amended independent Claim 16 and therefore incorporate the patentable features of amended Claim 16. Further, Claim 17 is cancelled by the above amendment and therefore Applicants consider the rejection of Claim 17 moot.

Amended Claim 16 is directed to a microprocessor. The microprocessor includes a first bank of execution units for executing instructions and a second bank of execution units for executing instructions. The microprocessor further includes a first register file, a second register file, and circuitry for enabling or disabling selected ones of read ports and write ports for each register file to control access by threads to the register files. The microprocessor has a single thread mode in which a single thread executes and a multi-thread mode in which multiple threads execute. The circuitry in the single thread mode enables the read and write ports for both the first register file and the second register file for access by the single thread. In the single thread mode a single register name is

renamed to refer to a first location in the first register file and a first location in the second register file. The Levy reference does not anticipate Claim 16 as amended.

The Levy reference discloses a microprocessor that allocates architectural registers from inactive context to active context for use as renaming registers by the active context. Nowhere does the Levy reference disclose that in a single-thread mode a single register name is renamed to refer to a first location in a first register file and a first location in a second register file. The Levy reference merely increases the number of renaming registers available to active context should there be inactive context. Nowhere does the Levy reference disclose the renaming of a first register name to refer to two register locations, one in a first register file and one in a second register file. Accordingly, the Levy reference does not anticipate amended Claim 16.

Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 16 and 18-20 under 35 U.S.C. §102(b).

CLAIM REJECTIONS UNDER 35 U.S.C. §103

Claims 4, 5, 7, 14, and 15 stand rejected under 35 U.S.C. §103(a). For ease of the discussion below relative to the rejections under 35 U.S.C. §103 each respective claim set is discussed separately below.

IIA. Rejection of Claims 4 and 5 Under 35 U.S.C. §103(a):

Claims 4 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy in view of U.S. Patent No. 5,900,025 of Sollars (hereinafter "Sollars"). Applicants respectfully traverse this rejection and contend that neither Levy nor Sollars, alone or in combination, detract from the patentability of Claims 4 and 5.

Claims 4 and 5 depend, directly or indirectly upon amended independent Claim 1 and therefore, incorporate the patentable features of amended Claim 1.

The Sollars reference is cited for teaching the use a number of control registers for controlling hardware and operation modes. The Sollars reference is also cited for teaching that computer systems have control registers for controlling system operations. Nevertheless, the Sollars reference fails to bridge the factual deficiencies of the Levy

reference. That is, the Sollars reference does not disclose a microprocessor that includes a single-thread mode in which a register name is renamed to refer to a first location in a first register file and to a first location in a second register file. Accordingly, neither Levy nor Sollars, alone or in combination, detract from the patentability of Claims 4 and 5.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 4 and 5 under 35 U.S.C. §103(a).

IIB. Rejection of Claim 14 Under 35 U.S.C. §103(a):

Claim 14 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy in view of Sollars. Applicants respectfully traverse this rejection and contend that neither Levy nor Sollars, alone or in combination, detract from the patentability of claim 14.

Claim 14 depends, directly or indirectly upon amended independent Claim 11 and therefore incorporates the patentable features of amended Claim 11.

The Sollars reference is cited for teaching the use of a number of control registers for controlling hardware and operation modes. The Sollars reference is also cited for teaching that all computers have such control registers for controlling system operations. Nevertheless, the Sollars reference fails to bridge the factual deficiencies of the Levy reference. More specifically, the Sollars reference fails to teach or suggest a method in a microprocessor having multiple registers that renames a register in a single-thread mode to refer to locations in each respective ones of multiple register sets. Hence, neither Levy nor Sollars, alone or in combination, detract from the patentability of Claim 14.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 14 under 35 U.S.C. §103(a).

IIC. Rejection of Claim 7 Under 35 U.S.C. §103(a):

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy in view of U.S. Patent No. 5,913,059 of Torii (hereinafter "Torii"). Applicants respectfully traverse this rejection and contend that neither Levy nor Torii, alone or in combination, detract from the patentability of Claim 7.

Claim 7 depends, directly or indirectly upon amended independent Claim 1 and therefore, incorporates the patentable features of amended Claim 1.

The Torii reference is cited for teaching a means for transferring data from one register file to another in a multi-threaded out of order system when a new thread is generated. Nevertheless, the Torii reference fails to bridge the factual deficiencies of the Levy reference. That is, the Torii reference does not teach or suggest a microprocessor having a single-thread mode where a register name is renamed to refer to a first location in a first register file and to a first location in a second register file. Hence, neither Levy nor Torii, alone or in combination, detract from the patentability of Claim 7.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 7 under 35 U.S.C. 35 U.S.C. §103(a).

IID. Rejection of Claim 15 Under 35 U.S.C. §103(a):

Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy in view of Torii. Applicants respectfully traverse this rejection and contend that neither Levy nor Torii, alone or in any combination, detract from the patentability of Claim 15.

Claim 15 depends, directly or indirectly upon amended independent Claim 11 and therefore incorporates the patentable features of amended Claim 11.

The Torii reference is cited for teaching a means for transferring data from one register file to another in a multi-threaded out of order system in an automatic manner when a new thread is generated to achieve coherence between register files with one register file copying contents to the other. Nevertheless, Torii fails to bridge the factual deficiencies of Levy for Torii does not teach or suggest a method performed in a microprocessor that includes a step when the microprocessor is in a single-thread mode of renaming a single register name to refer to a location in each respective ones of the multiple register sets of the microprocessor. As such, neither Levy nor Torii, alone or in combination, detract from the patentability of Claim 15.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 15 under 35 U.S.C. §103(a).

CONCLUSION

In light of the aforementioned amendments and arguments, Applicants contend that each of the Examiners rejections have been adequately addressed and the pending application is in condition for allowance.

Should the Examiner feel that a telephone conference with Applicants' attorney would expedite prosecution of this application, the Examiner is urged to contact the Applicants' attorney at (617) 227-7400.

Respectfully submitted,

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